**Rajeshwari MP**

#302,2ND Floor, C –block, Gagan vihar apartment, Ideal homes township, Rajarajeshwari nagar,

Bangalore- 560098 **Ph (M**):-9591860365 **Email**: [rajeswarimp.intel@gmail.com](mailto:rajeswarimp.intel@gmail.com)

**Entry level position in Development and Design/Testing, preferably in the IT sector**

**SYNOPSIS**

To work in a firm with a professional work driven environment where I can utilize and apply my knowledge, skills which would enable me as a fresh graduate to grow while fulfilling organizational goals.

**AREAS OF STREANT**

* Language: C++, C, Verilog, VHDL
* Presentation skills
* Strong decision making

**ACADEMIC QUALIFICATIONS**

* BE With specification in Electronics and Communication Engineering (2014) from VTU University Belgaum Karnataka with 58%
* 12th from board of pre-university education, Karnataka with 71.33%
* 10th from Karnataka secondary Education Examination Board with 89.28%

**TECHNICAL SKILLS**

**Operating systems:** windows xp/7

**Languages:**  Concepts in C and C++, Verilog, VHDL

**VLSI Designing**: FPGA Implementation

**ACADEMIC PROJECTS**

**PROJECT**

**Title: FPGA Implementation of optimized reversible multiplier**

**Duration:** 3 months **Team size:** 2

**Description:**

Reversible logic can play a significant role in computer domain. This logic can be applied in quantum computing, optical computing processing, DNA computing, and nanotechnology. One condition for reversibility of a computable model is that the number of input equate with the output. Reversible multiplier circuits are the circuits used frequently in computer system. For this reason, optimization in one reversible multiplier circuit can reduce its volume of hardware on one hand and increases the speed in a reversible system on the other hand. One of the important parameters that optimize a reversible circuit is reduction of delays in performance of circuit..

**Responsibility:**

* Design of 4X4 multiplier with delay reduction
* Design of 8x8 multiplier
* Design of 16x16 multiplier
* To implement on FPGA

**Personal Details**

Language known : English, Hindi, Kannada

Location Preference : Bangalore

Marital status : Single

Date of Birth : 05-06-1992